REMARKS/ARGUMENTS

Claims 31-42 are pending. Claims 31-40 were rejected under the judicially created doctrine of double patenting over claims 15-17 and 20 of U.S. Patent No. 6,678,807. Claims 36 and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Witt (U.S. Patent No. 6,141,747). Claim 31 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt and Tanenbaum. Applicants gratefully acknowledge the Office Action's indication that claims 41 and 42 are allowable. With regard to the double patenting rejection, Applicants submit the attached Terminal Disclaimer obviates the rejection.

Applicants respectfully traverse the Examiner's rejection because *Witt* does not teach or suggest all of the elements of the claims. Specifically, *Witt* does not teach a processor having a write combining buffer, where the processor authorizes store buffer forwarding by determining that: (1) the memory region associated with a load instruction matches a cache line address; and (2) the memory associated with store instructions completely covers the memory region associated with the load instruction, as found in embodiments of the present application.

The present application provides examples illustrating the erroneous behavior of store-forwarding operations in architectures similar to that of *Witt*. Summarizing those examples, if a given load operation is satisfied by store-forwarding from two different store operations, unpredictable results may occur in a multiprocessor environment if those two store operations are globally observed at different times. Embodiments of the present invention solve that problem, which *Witt* overlooks, by ensuring that *the memory requested by a load instruction matches a cache line address,* and by further requiring *the memory requested by a load instruction to be completely covered by memory associated with the store instructions from which the desired load data will be forwarded.*

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These two steps ensure that store buffer forwarding will be authorized only when the relevant data will be transmitted to memory in a single transaction, thereby ensuring data consistency in a multiprocessor environment. *Witt* overlooks the critical need to guarantee an atomic update of system memory in a multiprocessor architecture and *Witt* therefore fails to determine whether these two criteria are satisfied before permitting store-forwarding to occur.

In the Office Action, the Examiner indicated that *Witt* anticipates claims 36 and 40 because "[l]oad data may be forwarded from the store queue if the load data is stored therein, *which relates to the determining step as claimed* [col. 2, lines 12-14; here the matching of first and second memory regions is contemplated, and the covering of the second step by the first is realized and produces the forwarding of data as claimed]." Office Action at 5 (emphasis added). The Applicants respectfully disagree. Column 2, lines 12-14 state:

> "Advantageously, the load data may be forwarded from the store queue if the load data is stored therein."

As argued previously, rather than teach or suggest the determining steps as claimed, *Witt* merely describes forwarding the load data generically, and only *if it is available*. However, more importantly, the cited section does not describe either determining that: (1) the memory region associated with a load instruction matches a cache line address; or (2) the memory associated with store instructions completely covers the memory region associated with the load instruction, as *specifically recited* in claim 36.

The recent Office Action alleges that the *Witt* reference "teaches the determining steps in that the data is forwarded if the data is available based on the matching of memory regions, matching being that the first region "covers" the second region. Data is only forwarded if the data is available due to the determining by *Witt* that the regions overlap". Again, this assertion is

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unsupported by a reference to *Witt*. In order to be a proper 35 U.S.C. §102(e) rejection, the claimed limitations must be found in the cited reference. Applicants respectfully submit that the Office Action's assertions, absent support from the *Witt* reference itself, are inadequate to support a proper 35 U.S.C. §102(e) rejection.

For at least these reasons, Applicants respectfully assert that *Witt* does not teach or suggest the invention described by claims 36. As a result, *Witt* does not anticipate these claims. Accordingly, Applicants respectfully request withdrawal of these grounds of rejection. Independent claim 31 contains similar allowable limitations.

Tanenbaum fails to make up for the deficiencies of *Witt*. According to the Examiner, *Tanenbaum* teaches that computer hardware capabilities can be reproduced in software, and thus it would have been obvious to one skilled in the art to construct a software version of *Witt's* store-forwarding system. However, even if *Witt's* store-forwarding system were realized in software using *Tanenbaum* as a guide, the result still would not disclose the claimed invention. In particular, nothing in a *Witt-Tanenbaum* combination would teach or suggest store buffer forwarding only when the memory region associated with a load instruction matches a cache line address and when the memory associated with the relevant store instructions completely covers the memory region associated with the load instruction.

For at least all the above reasons, the Applicants respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

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Reply to Office Action dated: October 17, 2005

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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